List of reference symbols

No.	Technical component or Functional characteristic
100	Circuit layout of a Printed Circuit Board (PCBs) which is suitable for programming and configuration of two flash memories 114 and 116 (Flash-1, Flash-2) via a Boundary Scan (BSCAN) register 118 via JTAG interface 102 in accordance with Standard IEEE 1532, whereby the interface between the ASIC 108 and the second flash memory 116 (Flash-2) is formed by a part of the BSCAN register
102	JTAG interface of PCB 100 for input and output of standard bus signals TDI, TDO, TMS, TCK and TRST as well as for input of the control signals of the second application-specific integrated circuit 106 (ASIC-2)
104	first application-specific integrated circuit (ASIC-1) to accept the TDI signal via JTAG interface 102 and programming of the first flash memory 114 (Flash-1) via an interface in accordance with the IEEE 1149.1 Standard and control of the Field-Programmable Gate Array 112 (FPGA-1) via a configuration register 119a
106	second application-specific integrated circuit (ASIC-2) without configuration register, controllable via the Field-Programmable Gate Array 112 (FPGA-1)
108	third application-specific integrated circuit (ASIC-3) for programming the second Flash memory (Flash-2) via a BSCAN register 118 in accordance with the IEEE 1532 Standard
110	integrated circuit (IC) for output of the TDO signal via JTAG interface 102
112	Field-Programmable Gate Array (FPGA-1), for configuration controllable via a configuration register 119a

No.	Technical component or Functional characteristic
114	first flash memory (Flash-1), programmable with the aid of the first application-specific integrated circuit 104 (ASIC-1)
116	second flash memory (Flash-2), programmable with the aid of the third application-specific integrated circuit 108 (ASIC-3) via a BSCAN register 118
118	Boundary Scan (BSCAN) register, needed for programming the second flash memory 116 (Flash-2) with the aid of the third application-specific integrated circuit 108 (ASIC-3)
119a	Configuration register, needed for configuration of the Field-Programmable Gate Array 112 (FPGA-1)
119b	Configuration register, needed for programming the second flash memory 116 (Flash-2) with the aid of the third application-specific integrated circuit 108 (ASIC-3)
120	combined unit to be considered as a unit consisting of the third application-specific integrated circuit 108 (ASIC-3), the second flash memory to be programmed 116 (Flash-2), the configuration register 119b as well as the BSCAN register 118
200	reduced circuit layout of a Printed Circuit Board (PCBs) for programming and configuration of an integrated flash memory 116 (Flash-2) via a Boundary Scan (BSCAN) register 118 via JTAG interface 102 based on a Boundary Scan Description Language (BSDL) file in accordance with Standard IEEE 1532, whereby a configuration register 119b in accordance with IEEE Standard 1532 is connected to the output of the third application-specific integrated circuit 108 (ASIC-3)
202	fourth application-specific integrated circuit (ASIC-

No.	Technical component or Functional characteristic
	4) for output of the TDO signal via JTAG interface 102
204	combined cell of BSCAN registers 118, consisting of the interconnection of a capture cell 204a and a scan cell 204b
204a	Scan or capture cell of configuration register 119b for buffering configuration data or capture cell of BSCAN register 118 for buffering the programming data received form the third application-specific integrated circuit (ASIC-3)
204b	Scan or capture cell of BSCAN register 118, needed for controlling a control signal, address or data input of the second flash memory to be programmed 116 (Flash-2)
206	output-side operational amplifier with adjustable gain factor (VGA) at the output of the scan cell 204b of BSCAN registers 118 responsible for the generation of the relevant control, address or data signal
300	Detailed views of two exemplary embodiments of circuit layout 200 for connecting multiplexers 302a, 302b1/302b2, 302c and flip-flops 304, 306, 308 of a scan cell 204b of BSCAN registers 118 and a capture cell 204a of configuration register 119b for providing the control, data and address signals needed for programming the flash memory 116 (Flash-2) - Variant 1: Use of the first exemplary embodiment 302b1 of the output multiplexer (MUX2) - Variant 2: Use of the second exemplary embodiment 302b2 of the output multiplexer (MUX2) and use of configuration update flip-flops 310 (Conf UPD-FF) at the output of capture cells 204a of configuration register 119b
302a	Input multiplexer (MUX1) of a capture cell 204a of

No.	Technical component or Functional characteristic
	BSCAN register 118 for through connecting one of two input signals (DATA_IN, SCAN_IN) depending on a selection signal (SHIFT_DR) present at a control signal input (SEL)
302b	first variant of the output multiplexer (MUX2) of a scan cell 204b of BSCAN register 118 for through connecting one of two input signals (DATA_IN, Conf data) depending on a selection signal (MODE) present at a control signal input (SEL)
302b	second variant of the output multiplexer (MUX2) of a scan cell 204b of BSCAN register 118 for through connecting one of three input signals (DATA_IN, SCAN_OUT, Conf data) in depending on a selection signal (MODE) present at a control signal input (SEL)
302c	Output multiplexer (MUX) of a capture cell 204a of configuration register 119 for through connecting one of two input signals (SCAN_OUT, Conf. data) depending on a selection signal (UPD_DR) present at a control signal input (SEL)
304	Scan or capture flip-flop (Scan FF) of a capture cell 204a of BSCAN register 118, realized as an edge-triggered delay (D) flip-flop
306	Update flip-flop (UPD-FF) of a scan cell 204b of BSCAN register 118, realized as a edge-triggered delay (D) flip-flop with inverting clock signal input and a signal input for an ENABLE signal (UPD_DR BSCAN)
308	Configuration scan or configuration capture flip-flop (Conf Scan-FF) of a capture cell 204a of configuration register 119b, realized as a edge-triggered delay (D) flip-flop
310	Configuration update flip-flop (Conf UPD-FF) of a cap-

No.	Technical component or Functional characteristic
	ture cell 204a of configuration register 119b, realized as a edge-triggered delay (D) flip-flop with signal input for an ENABLE signal (UPD_DR CONF) with inverting clock signal input
TCK	Standard bus signal "Test Clock" of the Test Access Port (TAP) for clocking the TAP controller in accordance with IEEE Standard 1149.1
TDI	Standard bus signal "Test Data In" of the Test Access Port (TAP) for serial shifting in of data via JTAG interface 102 in accordance with IEEE Standard 1149.1
TDO	Standard bus signal "Test Data Out" of the Test Access Port (TAP) for serial shifting out of data via JTAG interface 102 in accordance with IEEE Standard 1149.1
TMS	Standard bus signal "Test Mode Select" of the Test Access Port (TAP) for switching over the states of the TAP controller in accordance with IEEE Standard 1149.1
TRST	Standard bus signal "Test Reset" of the Test Access Port (TAP) for asynchronous reset of the TAP controller in accordance with IEEE Standard 1149.1